

## Claims

- [c1] An integrated circuit (IC) comprising:
- an array of memory cells arranged in rows and columns;
  - an address bus for receiving addressing information;
  - a data-in path for receiving data during a write memory access;
  - a signal out path coupled to the memory array for outputting data during a read;
  - a data-out path coupled to the signal out path; and
  - a redundancy unit comprising,
    - at least one redundancy element having tag, address, and data portions, the tag portion indicates whether the redundancy element has been programmed for redundancy, the address portion contains a defective address if the redundancy element has been programmed for redundancy, and the data portion contains data associated with the defective address,
    - a control circuit for generating an active signal indicating that an access is associated with the defective address,
    - a read redundancy control circuit coupled to the output signal path and redundancy unit, and
    - a write redundancy control unit coupled to the data in path and redundancy unit.
- [c2] The IC of claim 1 wherein the memory cells comprise SRAM cells.
- [c3] The IC of claim 1 wherein the memory cells comprise DRAM cells.
- [c4] The IC of claim 1 wherein the memory cells comprise multi-port DRAM cells.
- [c5] The IC of claim 1 wherein the memory cells comprise multi-port DRAM cells with SRAM functionality.
- [c6] The IC of claim 1 wherein the redundancy unit comprises a plurality of redundancy elements.
- [c7] The IC of claim 6 wherein the control circuit comprises a comparator, the comparator compares the address of the memory access from the address bus and addresses in the redundancy elements and generates the active signal if

there is a match with one address in one of the redundancy elements.

- [c8] The IC of claim 7 wherein the read redundancy control circuit is activated when the active signal is generated and the memory access is a read access.
- [c9] The IC of claim 8 wherein the read redundancy control circuit comprises:  
a first read control switch coupled to the output signal path and data-out path;  
and  
a second read control switch coupled to the redundancy unit and data-out path,  
when the read redundancy control circuit is activated, the first switch is disabled to decouple the output signal path from the data-out path and the second switch is enabled to couple the redundancy unit to the data-out path; and  
when the read redundancy control circuit is deactivated, the first switch is enabled to couple the output signal path from the data-out path and the second switch is disabled to decouple the redundancy unit to the data-out path.
- [c10] The IC of claim 7 wherein the write redundancy control circuit is activated when the active signal is generated and the memory access is a write access.
- [c11] The IC of claim 10 wherein the write redundancy control circuit comprises:  
a write control switch coupled to the data-in path and the redundancy unit;  
when the write redundancy control circuit is activated, the write control switch is enabled to couple the data-in path to the redundancy unit; and  
when the write redundancy control circuit is deactivated, the write control switch is disabled to decouple the data-in path from the redundancy unit.
- [c12] The IC of claim 10 wherein the write redundancy control circuit comprises:  
a first write control switch coupled to the data-in path and the redundancy unit;  
a second write control switch coupled to the data-in path and the array;  
when the write redundancy control circuit is activated, the first write control switch is enabled to couple the data-in path to the redundancy unit and the second write control switch is disabled to decouple the data-in path from the array; and  
when the write redundancy control circuit is deactivated, the first write control switch is disabled to decouple the data-in path from the redundancy unit and

the second write control switch is enabled to couple the data-in path to the array.

- [c13] The IC of claim 1 wherein the control circuit comprises a comparator, the comparator compares the address of the memory access from the address bus and address in the at least one redundancy element and generates the active signal if there is a match with one address in one of the redundancy element.
- [c14] The IC of claim 13 wherein the read redundancy control circuit is activated when the active signal is generated and the memory access is a read access.
- [c15] The IC of claim 14 wherein the read redundancy control circuit comprises:  
a first read control switch coupled to the output signal path and data-out path;  
a second read control switch coupled to the redundancy unit and data-out path;  
when the read redundancy control circuit is activated, the first switch is disabled to decouple the output signal path from the data-out path and the second switch is enabled to couple the redundancy unit to the data-out path; and  
when the read redundancy control circuit is deactivated, the first switch is enabled to couple the output signal path from the data-out path and the second switch is disabled to decouple the redundancy unit to the data-out path.
- [c16] The IC of claim 13 wherein the write redundancy control circuit is activated when the active signal is generated and the memory access is a write access.
- [c17] The IC of claim 16 wherein the write redundancy control circuit comprises:  
a write control switch coupled to the data-in path and the redundancy unit;  
when the write redundancy control circuit is activated, the write control switch is enabled to couple the data-in path to the redundancy unit; and  
when the write redundancy control circuit is deactivated, the write control switch is disabled to decouple the data-in path from the redundancy unit.
- [c18] The IC of claim 16 wherein the write redundancy control circuit comprises:  
a first write control switch coupled to the data-in path and the redundancy unit;  
a second write control switch coupled to the data-in path and the array;  
when the write redundancy control circuit is activated, the first write control switch is enabled to couple the data-in path to the redundancy unit and the

second write control switch is disabled to decouple the data-in path from the array; and

when the write redundancy control circuit is deactivated, the first write control switch is disabled to decouple the data-in path from the redundancy unit and the second write control switch is enabled to couple the data-in path to the array.

- [c19] The IC of claim 1 further comprising a test control unit performing a test to determine defective addresses.
- [c20] The IC of claim 19, wherein the test is performed during the initialization of the IC.